

GAIN VARIABLE AMPLIFIER

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Abstract of JP4160810

PURPOSE: To decrease the degree of a narrowed dynamic range by a degree of omission of a buffer circuit by controlling directly a base voltage of a DC voltage level control transistor (TR) with a gain control voltage.

CONSTITUTION: A voltage $V_{GC} < + >$ fed to a positive gain control signal input terminal 1a in a gain control signal V_{GC} is higher than a $V_{GC} < - >$ fed to a negative gain control signal input terminal 1b, since a current flowing to a constant current source 2 is constant, a collector current of a 1st TR Q1 increases and a collector current of a 2nd TR Q2 decreases. In this case, a current flowing from a constant current source 3 being a component of a voltage source 10 flows while being branched into a path from the 2nd TR Q2 to the constant current source 2 and a path of a resistor R1, and the current sum is constant. Thus, a buffer circuit employing an NPN TR is omitted and the degree of a narrowed dynamic range in an output signal is suppressed when a power supply voltage applies to a power voltage terminal is low.

